Part A. PERSONAL INFORMATION

		CV date	27/03/21

First and Family name	JULIO VILLALBA MORENO		
Social Security, Passport, ID number		Age	
Researcher codes	WoS Researcher ID *(*)*		
	SCOPUS Author ID*(*)*	7006410722	
	Open Researcher and Contributor ID (ORCID) **	0000-0001-8557-3876	

(*) At least one of these is mandatory
(**) Mandatory

A.1. Current position

Name of University/Institution	Universidad de Málaga		
Department	Arquitectura de Computadores		
Address and Country	Málaga, Andalucía, España		
Phone number	+34952132787	E-mail	jvillalba@uma.es
Current position	Catedrático de Universidad	From	2007
Key words			

A.2. Education

PhD	University	Year
Dr. Informatica	Malaga	1995
Lic. Fisica	Granada	1986

Tramos de docencia: 6; **Last**: 2014-2019
Tramos de Investigación (Sexenios): 4; **Last:** 2014-2020

Total JCR articles: 21 **; Q1 JCR articles: 10**
H-index: 12 ;**Total citations**:453 (Scopus)
Thesis supervised: 6

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

Julio Villalba-Moreno received the B.S. degree in Physics Sciences in 1986 from the University of Granada and PhD. degree in Computer Science from the University of Málaga (SPAIN). At present he is a full professor in the Department of Computer Architecture in the Univ. Malaga.

From mid 1986 to late 1991 he worked as a design engineer in the Research and Development Department of Fujitsu Spain (R&D Digital Signal Processing group). From late 1986 to 1993 he was an Assistant professor, from 1993 to 2007 he was an Associate Professor and from 2007 to nowadays he is a Full professor, all in the Department of Computer Architecture of the University of Malaga.

He was a Visiting Scholar in the Department of Electrical Engineering and Computer Science of the University of California at Irvine in 1996, 2003, 2004 and 2005 for a total of one year. During these stays he did research in computer arithmetic algorithm in collaboration with Professor Tomas Lang.

From 2006 to nowadays he is a member of the Program Committee of the IEEE International Symposium on Computer Arithmetic. He also belongs to the IEEE-1788 working group Standardization of Interval arithmetic. He is the leader of the group "application specific architectures and computer arithmetic" in the Dept. of Computer Architecture.

Regarding the transfer of research results, he is one of the inventor of 5 Spanish patents granted to the University of Malaga in 2015 with examination. In addition, these patents were extended by PCT and in USA.

He was an associate Editor of the IEEE Transactions on Computers from July 2011 to June 2015 the IEEE Transactions on Emerging Topics in Computing from September 2015 to August 2018 and was serving as a Program Chair in the 22nd IEEE International Symposium on Computer Arithmetic (Lyon, France, June 22-24, 2015). Currently he also belongs to the Steering Committee of the IEEE Symposium on Computer Arithmetic since 2015.

His research interests are computer arithmetic, interval arithmetic, decimal arithmetic, application specific architectures and processors, FPGA designs, hardware design for image processing and digital signal processing, embedded systems, multimedia extension of processors.

Part C. RELEVANT MERITS

C.1. Publications (including books):

1. Francisco J. Jaime, Miguel.A. Sánchez, Javier Hormigo, Julio Villalba, Emilio L. Zapata, Enhanced Scaling-Free CORDIC,IEEE Transactions on Circuits and Systems I, vol. 57, num. 7, pp. 1654-1662, 2010
2. Francisco J. Jaime, Miguel.A. Sánchez, Javier Hormigo, Julio Villalba, Emilio L. Zapata, High Speed Algorirhms and Architectures for Range Reduction Computation , IEEE Transactions on Very Largue Scale Integration (VLSI) Systems , vol. 19, num. 3, pp. 512-516, 2011
3. Julio Villalba, Tomas Lang y Javier Hormigo, Radix-2 Multioperand and Multiformat Streaming On-line Addition , IEEE Transactions on Computers, vol 61, num 6, pg. 790-803, 2012
4. Vazquez, A. Villalba, J. Antelo, E. Zapata, E., Redundant Floating Point Decimal CORDIC Algorithm , IEEE Transactions on Computers, vol 61, num 11, pg. 1551 – 1562, 2012
5. J. Hormigo, J. Villalba, E. Zapata, E. , Multi-operand Redundant Adders on FPGAs, Transactions on Computers, Digital Object Identifier: 10.1109/TC.2012.168, vol 62, num 10, 2013
6. J. Hormigo, J. Villalba, Measuring Improvement When Using HUB Formats to Implement Floating-Point Systems Under Round-to-Nearest, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, DOI: 10.1109/TVLSI.2015.2502318, vol 24, num. 6, pp. 2369-2377, june 2016
7. J. Hormigo, J. Villalba, New Formats for Computing with Real-Numbers under Round-to-Nearest, IEEE Transactions on Computers, vol 99, Digital Object Identifier: 10.1109/TC.2015.2479623, vol. 65, num 7, pages 2158 - 2168, 2016
8. C. Garcia Vega; S. Gonzalez Navarro; P. Balboa-La Chica; J. Villalba. , Decimal Multiformat Online Addition, IEEE Transactions on Computers, Digital Object Identifier: 10.1109/TC.2016.2516009, vol. 65, num 10, pages 3203 – 3209, 2016
9. J. Hormigo, J. Villalba., HUB-Floating-Point for improving FPGA implementations of DSP Applications , IEEE Transactions on Circuits and Systems II, vol 64 , num 3, pages 319-323, March 2017
10. Julio Villalba-Moreno, Javier Hormigo, Sonia González. , Unbiased Rounding for HUB Floating-Point Addition. IEEE Transactions on Computers, Digital Object Identifier: 10.1109/TC.2018.2807429, vol., 67, num 9 pages 1359-1365 , 2018, September 2018
11. Julio Villalba-Moreno, Javier Hormigo, Sonia González. Fast HUB Floating-point Adder for FPGA, IEEE Transactions on Circuits and Systems II: Express Briefs, Digital Object Identifier: 10.1109/TCSII.2018.2873194, vol. 66, , num 6 pages 1028-1032 , June 2019,

12. J. Villalba J. Hormigo , Optimizing DSP Circuits by a New Family of Arithmetic Operators , 48th Asilomar Conference on Signals, Systems and Computers , Proceedings pp 871-875, Asilomar, California, USA, 2-5 Nov 2014

13. J. Hormigo , J. Villalba , Simplified Floating-Point Units for High Dynamic Range Image and Video Systems ,19th IEEE International Symposium on Consumer Electronics ISCE 2015 , Madrid, Spain, 24-26 Jun 2015

14. J. Villalba, Digit Recurrence Floating-Point Division under HUB format, 23th IEEE Symposium on Computer Arithmetic ARITH23 , Proceedings pp 79-86, Silicon Valley, Califorina (USA), 10-13 Jul 2016

15. J. Villalba, J. Hormigo, Floating Point Square Root under HUB Format, International Conference on Computer Design ICCD 2017, Proceedings pp 447-454, Boston, Massachusetts (USA), 5-8 Nov. 2017

16. J. Villalba, J. Hormigo, F. Jaime , Reproducible summation under HUB format, 26th International Symposium on Computer Arithmetic - ARITH 2019, Proceedings pp 38-45, Kyoto, Japón, 10-12 Jun. 2019

17. Julio Villalba, Javier Hormigo, Sonia Gonzalez Navarro, Floating–Point Fused Multiply–Add under HUB Format, IEEE 27th Symposium on Computer Arithmetic - ARITH 2020, Proceedings pp 1-8, Portland, Oregon (USA) online by COVID19, 2020

C.2. Research projects and grant

1. TIN2016-80920-R. Arquitecturas de altas prestaciones para aplicaciones intensivas en datos. MINECO. Plata-González, Oscar (Universidad de Málaga). 2016-2019. 405.471 EUR.

2. TIN2013-42253-P. "Arquitecturas, Compiladores y Aplicaciones en Multiprocesadores", MINECO, IP: Emilio López Zapata, Universidad de Málaga, 2014-2016. 207.878 EUR. Investigador.

3. TIN2010-16144. Arquitecturas, Compiladores y Aplicaciones en Multiprocesadores. 2011-2013. ,IP: López-Zapata, Emilio (Universidad de Málaga). 2011-2015. 610.082 EUR. Investigador.

4. TIN2006-01078. Arquitecturas, Compiladores y Aplicaciones en Multiprocesadores. MEC,IP: López-Zapata, Emilio (Universidad de Málaga). 2006-2011. 1028500 EUR. Investigador.

5. TIN2006-01078. Arquitecturas, Compiladores y Aplicaciones en Multiprocesadores. MEC,IP: López-Zapata, Emilio (Universidad de Málaga). 2006-2011. 1028500 EUR. Investigador.

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C.3. Contracts

C.4. Patents

1. Hormigo, Javier; Villalba-Moreno, Julio. Multiplicadores coma flotante y conversores asociados, ES2546895B2, 2015.

2. Hormigo, Javier; Villalba-Moreno, Julio. Dispositivos coma flotante y conversores, ES2546898B2, 2015.

3. Hormigo, Javier; Villalba-Moreno, Julio. Sumadores coma flotante y conversores, ES2546916B2, 2015.

4. Hormigo, Javier; Villalba-Moreno, Julio. Unidades aritméticas en coma fija y conversores asociados, ES2546915B2, 2015.

5. Hormigo, Javier; Villalba-Moreno, Julio. Dispositivos para operaciones de multiplicación-suma fusionadas en coma flotante y conversores asociados, ES2546899B2, 2015.

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C.5 PhD Thesis supervised

1. Carlos García Vega, "Variable Radix Online Decimal Arithmetic", Universidad de Málaga, 2017

2. Manuel Agustin Ortiz Lopez, "Uso eficiente de aritmética redundante en FPGAs", Universidad de Córdoba, 2013.

3. Francisco José Jaime Rodríguez, "Hardware solutions for range reduction and elementary functions computation, Universidad de Málaga, 2011

. C.6 Participation in editorial committees at international journals and conferences

1. Program Chair at the 22rd IEEE Symposium on Computer Arithmetic. 2015

2. Associate editor of the Journal "IEEE transactions on Computer Arithmetic from July 2011 to June 2015

3. Associate editor of the Journal "IEEE transactions on Emerging Topics in Computing" from September 2015 to June 2018

4. Program Committee Member of the IEEE Symposium on Computer Arithmetic. 2006-nowadays

5. Member of the Steering Committee of the IEEE Symposium on Computer Arithmetic from 2015 to nowadays